In the claims:

Claims 1 to 9 (canceled)

Claim 10 (currently amended) A transistor which comprises:

(a) a semiconductor substrate having first and second spaced apart source/drain regions therein; and

(b) a channel region between said source/drain regions in said substrate having a relatively low V_T central region between said source/drain regions and relatively high controlling V_T regions adjacent to said source/drain regions, said channel region having an implanted one of a positive or negative V_T dopant intermediate said source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent said source/drain regions, the opposite of said dopant in said central region;

where controlling V_T is defined as that region which is the least conducting region and thus controls the current flow.

Claims 11 to 24 (canceled)

Claim 25 (previously presented) The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

Claim 26 (canceled)